

EE141 Review What Have We Learnt?

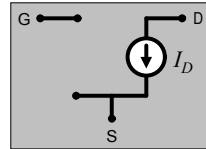
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The MOSFET – ID

$$V_{DS} > V_{GS} - V_T$$

Saturation:

$$I_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$$



$$V_{DS} < V_{GS} - V_T$$

Resistive:

$$I_D = k'_n \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

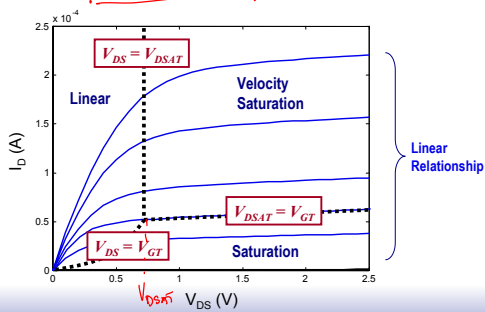
with

$$V_T = V_{T0} + \gamma \cdot (\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|})$$

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Regions of Operation – Simplified

□ Define $V_{GT} = V_{GS} - V_T$ $V_{DSAT} \approx L \cdot \xi_c$



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A Unified Model for Manual Analysis

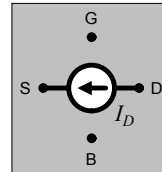
$$\text{define } V_{GT} = V_{GS} - V_T$$

for $V_{GT} \leq 0$: $I_D = 0$

for $V_{GT} \geq 0$:

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{\min} - \frac{V_{\min}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})$$

with $V_{\min} = \min(V_{GT}, V_{DS}, V_{DSAT})$



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Capacitive Device Model

□ Gate-Channel Capacitance

- $C_{GC} = C_{ox} \cdot W \cdot L_{eff}$ (Off, Linear)
- $C_{GC} = (2/3) \cdot C_{ox} \cdot W \cdot L_{eff}$ (Saturation)

$1/2$ to G-S $1/2$ to G-D
 100% to G-S 0% to G-D

□ Gate Overlap Capacitance

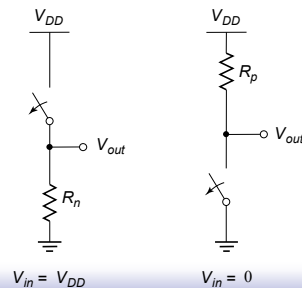
- $C_{GSO} = C_{GDO} = C_O \cdot W$ (Always)

□ Junction/Diffusion Capacitance

- $C_{diff} = C_j \cdot L_S \cdot W + C_{jsw} (2L_S + W)$ (Always)

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CMOS Inverter First-Order DC Analysis



$$\begin{aligned} V_{OL} &= 0 \\ V_{OH} &= V_{DD} \\ V_M &= f(R_n, R_p) \end{aligned}$$

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Diagram illustrating the definition of Noise Margin (NM) for a digital circuit.

The diagram shows a signal transition from "1" to "0" through a gate. The output of the gate (Stage M) is connected to the input of the next gate (Stage M+1).

The output voltage levels are V_{OH} (high) and V_{OL} (low). The input voltage levels are V_{IH} (high) and V_{IL} (low).

The noise margin high (NM_H) is the difference between V_{OH} and V_{IH} .

The noise margin low (NM_L) is the difference between V_{OL} and V_{IL} .

A graph shows the transfer characteristics of the gates, with V_{IL} and V_{IH} marked on the input axis.

The figure consists of two side-by-side plots of output voltage $V_{out}(V)$ versus input voltage $V_{in}(V)$ for a CMOS inverter. Both plots have axes ranging from 0 to 2.5 V.

The left plot is labeled "Symmetrical". It shows three curves: a red curve labeled "Wider PMOS" which is shifted to the right, and a blue curve labeled "Wider NMOS" which is shifted to the left. The curves are symmetric about $V_{in} = V_{out} = 1.25$ V.

The right plot is labeled "Nominal". It shows four curves: a red curve labeled "Fast PMOS", a blue curve labeled "Slow NMOS", a green curve labeled "Fast NMOS", and a purple curve labeled "Slow PMOS". The red and blue curves are shifted to the right, while the green and purple curves are shifted to the left. The curves are not symmetric about $V_{in} = V_{out} = 1.25$ V.

Figure 1 illustrates the small-signal equivalent circuit and the load line for a MOSFET in common-source configuration. The left part shows the equivalent circuit with a dependent current source $g_m v_{gs}$ in parallel with r_{ds} , and a load resistor R_{on} in series with the drain. The gate is biased at $V_{GS} \geq V_T$. The right part shows the I_D vs V_{DS} characteristic curve. The load line is a dashed line from the origin with slope $1/R_{on}$. The Q-point is at $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}/2$. The small-signal output resistance $R_{eq} = \frac{1}{2} \cdot (R_0 + R_{mid})$ is indicated by the slope of the tangent at the Q-point.

The diagram illustrates the Miller effect and Fanout analysis for a CMOS inverter. It is divided into two main parts: a detailed circuit model and a simplified model.

Miller Effect Analysis:

- 1 Miller effect:** Points to the input node of the inverter, where the input voltage V_{in} is applied. The input capacitance is C_{gs12} .
- 2 Reverse biased junction:** Points to the source-drain junction of the PMOS transistor (M2), which is reverse-biased.
- 3 Off $\rightarrow$ Sat (M_4) Lin (M_3):** Points to the PMOS transistor (M4) in the fanout stage, which is in saturation.
- 4 No Miller effect:** Points to the NMOS transistor (M3) in the fanout stage, which is in the linear region.

Fanout: The output of the first inverter is connected to the input of a second inverter, which is shaded gray. The second inverter has PMOS transistor M4 and NMOS transistor M3. Its input capacitance is C_{gs1} and its output is V_{out2} .

Simplified Model:

The simplified model shows a single inverter with input V_{in} and output V_{out} . The output is connected to a load capacitance C_L to ground. The output voltage is V_{out} .

Computing the Capacitances

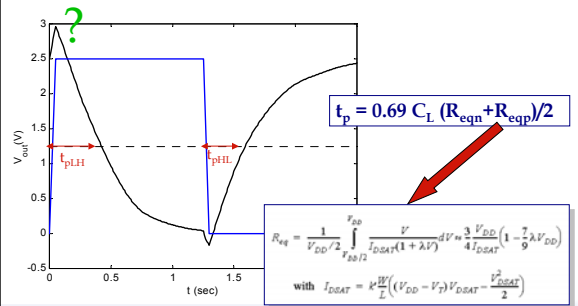
- ② Reverse biased junction Miller effect

Capacitor	Expression
C_{gd1}	$2 \cdot CGD0 \cdot W_n$
C_{gd2}	$2 \cdot CGD0 \cdot W_p$
C_{db1}	$K_{eqn} (AD_n \cdot CJ + PD_n \cdot CJSW)$
C_{db2}	$K_{eqn} (AD_p \cdot CJ + PD_p \cdot CJSW)$
C_{g3}	$C_0 \cdot W_n + 4 \cdot C_{ox} \cdot W_n \cdot L_n$ (Lin*)
C_{g4}	$C_0 \cdot W_p + 4 \cdot C_{ox} \cdot W_p \cdot L_p$ (Off → Sat*)
C_w	From Extraction
C_L	Σ

* assuming HL transition at V_{out}

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Propagation Delay



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Power in CMOS

- Switching power
 - Charging/Discharging capacitors
- Leakage power
 - Transistors are imperfect switches
 - Junction diodes
- Short-circuit power
 - Both pull-up and pull-down on during transition

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Dynamic (Switching) Power

- Energy consumed in N cycles, E_N :

$$E_N = C_L \cdot V_{DD}^2 \cdot n_{0 \rightarrow 1}$$

$n_{0 \rightarrow 1}$ – number of 0→1 transitions in N cycles

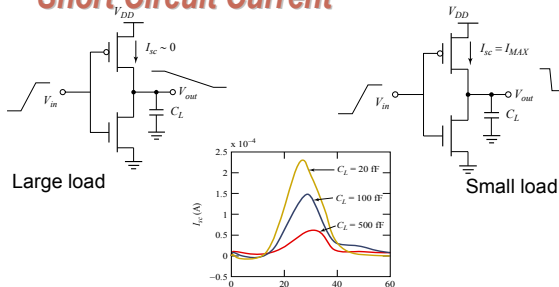
$$P_{avg} = \lim_{N \rightarrow \infty} \frac{E_N}{N} \cdot f = \left(\lim_{N \rightarrow \infty} \frac{n_{0 \rightarrow 1}}{N} \right) \cdot C_L \cdot V_{DD}^2 \cdot f$$

$$\alpha_{0 \rightarrow 1} = \lim_{N \rightarrow \infty} \frac{n_{0 \rightarrow 1}}{N} \cdot f$$

$$P_{avg} = \alpha_{0 \rightarrow 1} \cdot C_L \cdot V_{DD}^2 \cdot f$$

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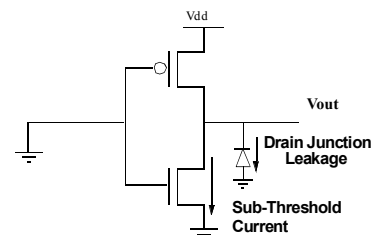
Short Circuit Current



- Short circuit current is usually well controlled

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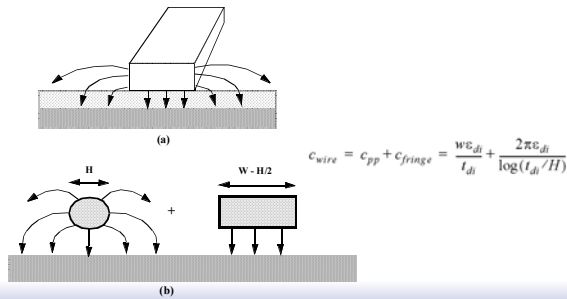
Transistor Leakage



Sub-threshold current one of most compelling issues in low-energy circuit design!

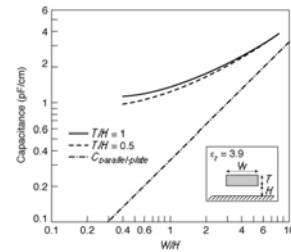
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WIRE: Fringing and Parallel Plate Capacitance



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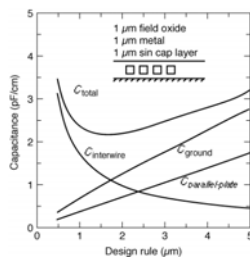
Fringing versus Parallel Plate



(from [Bakoglu89])

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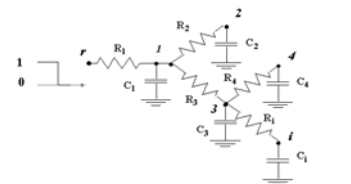
Impact of Interwire Capacitance



(from [Bakoglu89])

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The Lumped RC-Model The Elmore Delay

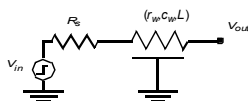


$$R_{ik} = \sum R_j \Rightarrow (R_j \in [\text{path}(s \rightarrow i) \cap \text{path}(s \rightarrow k)])$$

$$\tau_{Di} = \sum_{k=1}^N C_k R_{ik}$$

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Driving an RC-line

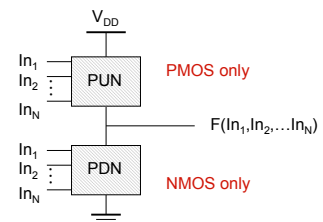


$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

$$t_p = 0.69 R_s C_w + 0.38 R_w C_w$$

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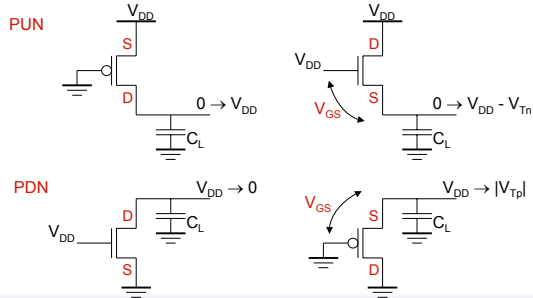
Logic Circuits Static Complementary CMOS



PUN and PDN are dual logic networks
 PUN and PDN functions are complementary

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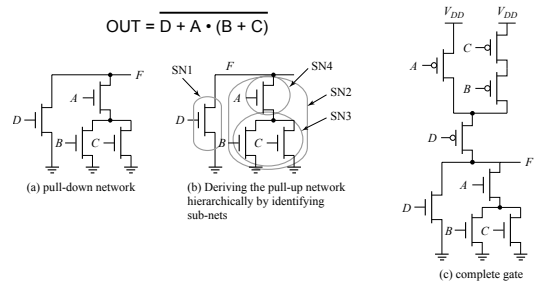
Threshold Drops



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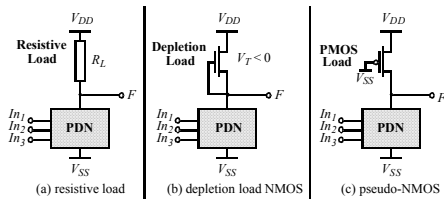
Constructing a Complex Gate

$$\text{OUT} = \overline{D + A \cdot (B + C)}$$



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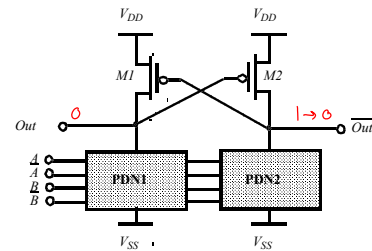
Ratioed Logic



Goal: to reduce the number of devices over complementary CMOS

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DCVSL

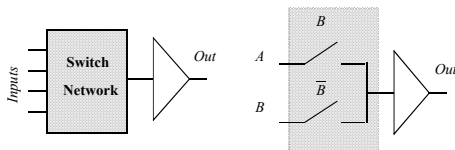


Differential Cascode Voltage Switch Logic (DCVSL)

Cascode at colcode

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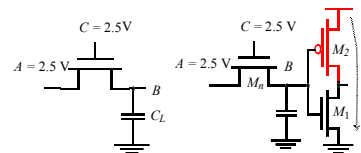
Pass-Transistor Logic



- N transistors
- No static consumption

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NMOS-only Switch



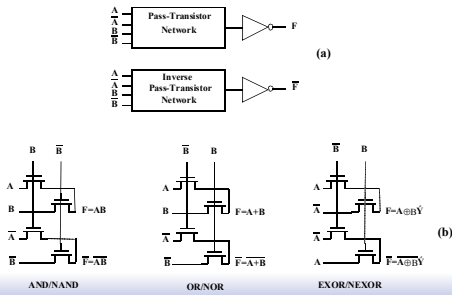
V_B does not pull up to 2.5V, but $2.5V - V_{TN}$

Threshold voltage loss causes static power consumption

NMOS has higher threshold than PMOS (body effect)

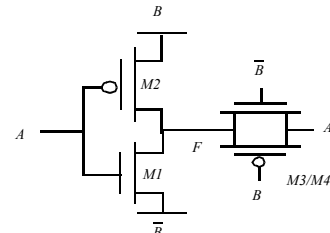
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Complementary Pass Transistor Logic



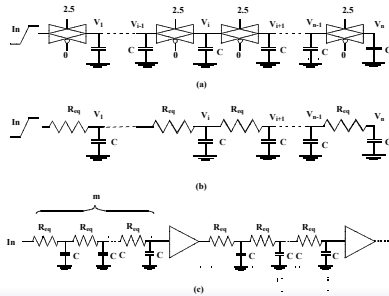
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Transmission Gate XOR



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Delay in Transmission Gate Networks



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Delay Optimization

• Delay of RC chain

$$t_p = 0.69 \sum_{k=0}^n CR_{eq} k = 0.69 CR_{eq} \frac{n(n+1)}{2}$$

• Delay of Buffered Chain

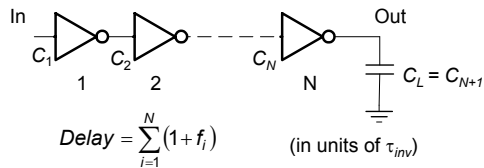
$$t_p = 0.69 \left[\frac{n}{m} CR_{eq} \frac{m(m+1)}{2} \right] + \left(\frac{n}{m} - 1 \right) t_{buf}$$

$$= 0.69 \left[CR_{eq} \frac{n(m+1)}{2} \right] + \left(\frac{n}{m} - 1 \right) t_{buf}$$

$$m_{opt} = 1.7 \sqrt{\frac{t_{buf}}{CR_{eq}}}$$

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Sizing for Speed: Buffer Example



For given N : $C_{i+1}/C_i = C_i/C_{i-1}$

To find N : $C_{i+1}/C_i \sim 4$

How to generalize this to any logic path?

$$f_i = C_{i+1}/C_i$$

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Logical Effort

$$Delay = k \cdot R_{unit} C_{unit} \left(1 + \frac{C_L}{\gamma C_{in}} \right)$$

$$= \tau(p + g \cdot f)$$

p – intrinsic delay ($3kR_{unit}C_{unit}\gamma$) – gate parameter $\neq f(W)$

g – logical effort ($kR_{unit}C_{unit}$) – gate parameter $\neq f(W)$

f – electrical effort (effective fanout)

Normalize everything to an inverter:

$$g_{inv} = 1, p_{inv} = 1$$

Divide everything by τ_{inv}

(everything is measured in unit delays τ_{inv})

Assume $\gamma = 1$.

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Multistage Networks

$$Delay = \sum_{i=1}^N (p_i + g_i \cdot f_i)$$

Stage effort: $h_i = g_i f_i$

Path electrical effort: $F = C_{out}/C_{in}$

Path logical effort: $G = g_1 g_2 \dots g_N$

Branching effort: $B = b_1 b_2 \dots b_N$

Path effort: $H = GFB$

Path delay $D = \sum d_i = \sum p_i + \sum h_i$

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Optimum Effort per Stage

When each stage bears the same effort:

$$\hat{h}^N = H$$

$$\hat{h} = \sqrt[N]{H}$$

Stage efforts: $g_1 f_1 = g_2 f_2 = \dots = g_N f_N$

Effective fanout of each stage: $f_i = \hat{h}/g_i$

Minimum path delay

$$\hat{D} = \sum (g_i f_i + p_i) = NH^{1/N} + P$$

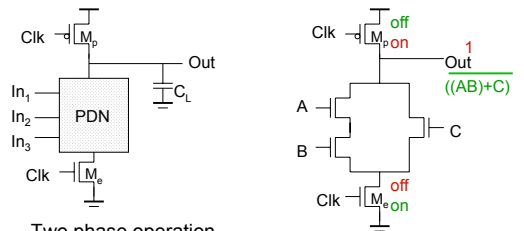
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Logical Effort Summary

	Stage	Path
Logical Effort	g	$G = \prod g_i$
Electrical Effort	$F = C_{out}/C_{in}$	$F = C_{out}/C_{in}$
Branching Effort	b	$B = \prod b_i$
Effort	$h = gf$	$H = GFB$
Effort Delay	t	$D_H = \sum h_i$
Number of Stages	1	N
Parasitic Delay	p	$P = \sum p_i$
Delay	$d = h + p$	$D = D_H + P$

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Dynamic Gate



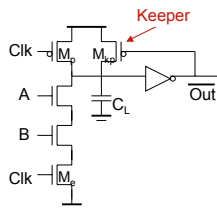
Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)

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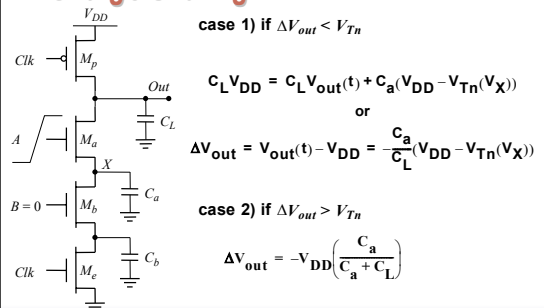
Solution to Charge Leakage



Same approach as level restorer for pass-transistor logic

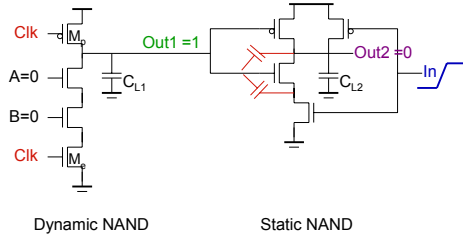
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Charge Sharing



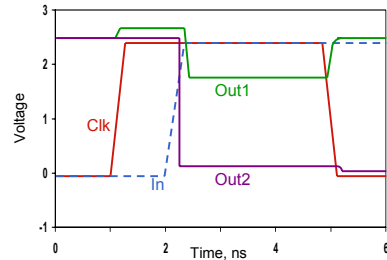
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Issues in Dynamic Design 3: Backgate Coupling



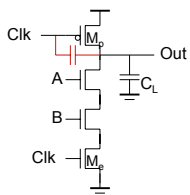
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Backgate Coupling Effect



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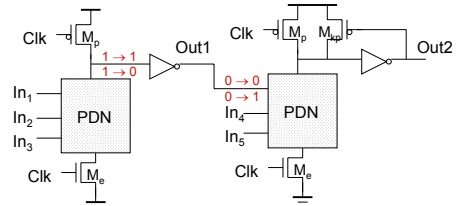
Issues in Dynamic Design 4: Clock Feedthrough



Coupling between Out and Clk input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above V_{DD} . The fast rising (and falling edges) of the clock **couple** to Out.

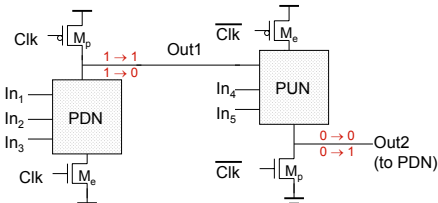
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Domino Logic



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np-CMOS

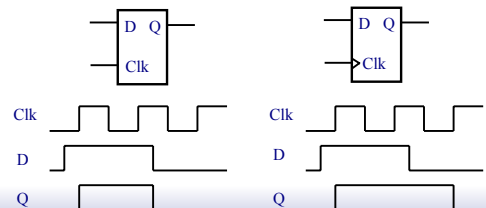


Only $0 \rightarrow 1$ transitions allowed at inputs of PDN
Only $1 \rightarrow 0$ transitions allowed at inputs of PUN

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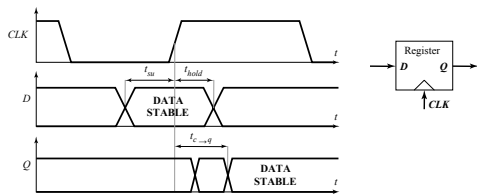
Sequential Logic Latch versus Register

- Latch – level-sensitive
clock is low – hold mode
clock is high – transparent
- Register – edge-triggered
stores data when clock rises



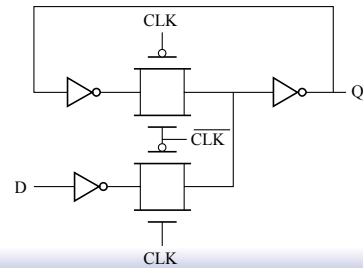
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Timing Definitions



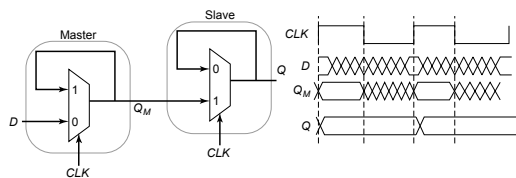
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Mux-Based Latch



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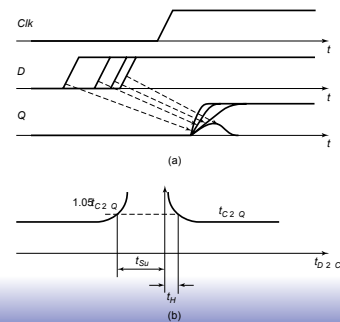
Master-Slave (Edge-Triggered) Register



Two opposite latches trigger on edge
Also called master-slave latch pair

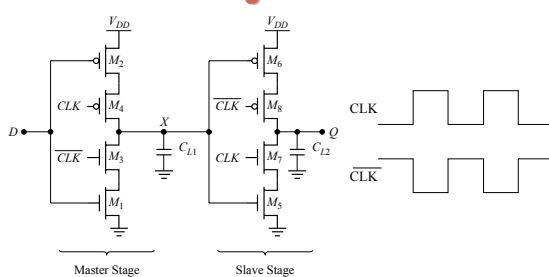
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More Precise Setup Time



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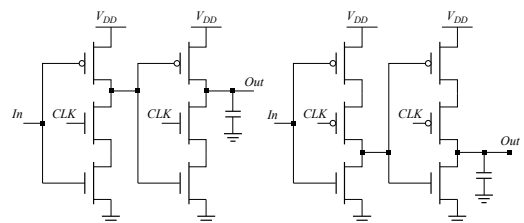
Other Latches/Registers: C²MOS



Keepers should be added to staticize

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Other Latches/Registers: TSPC



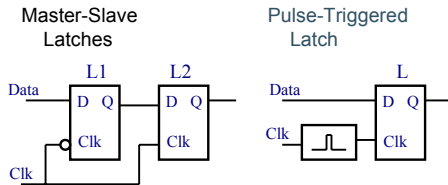
Positive latch
(transparent when CLK = 1)

Negative latch
(transparent when CLK = 0)

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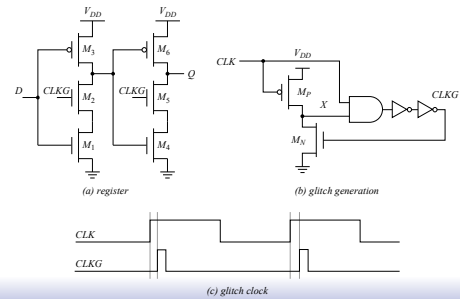
Pulse-Triggered Latches

Ways to design an edge-triggered sequential cell:



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Pulsed Latches



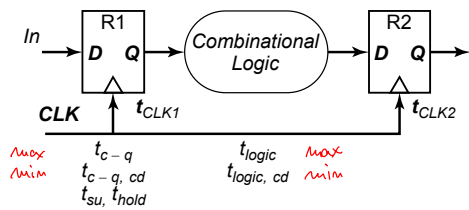
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Other Sequential Circuits

- Schmitt Trigger
- Monostable Multivibrators
- Astable Multivibrators

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Timing Constraints

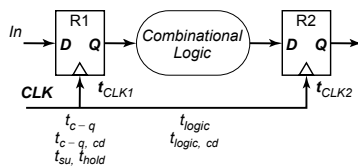


$$\text{Cycle time: } T_{\text{CLK}} > t_{c-q} + t_{\text{logic}} + t_{\text{su}}$$

$$\text{Race margin: } t_{\text{hold}} < t_{c-q, cd} + t_{\text{logic}, cd}$$

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Timing Constraints



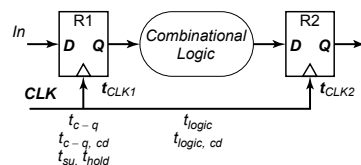
Minimum cycle time:

$$T + \delta = t_{c-q} + t_{\text{logic}} + t_{\text{su}}$$

Worst case is when receiving edge arrives early (negative δ)

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Timing Constraints



Hold time constraint:

$$t_{(c-q, cd)} + t_{(\text{logic}, cd)} > t_{\text{hold}} + \delta$$

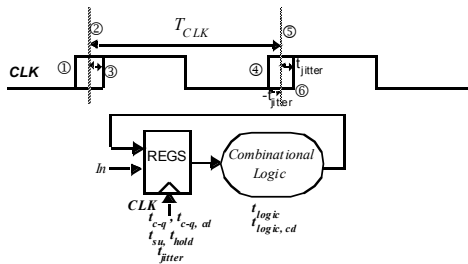
Worst case is when receiving edge arrives late

Race between data and clock

Negative skew: system NEVER FAILS!

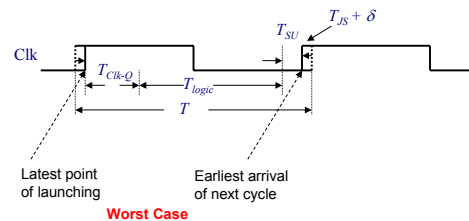
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Impact of Jitter



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Longest Logic Path in Edge-Triggered Systems



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Clock Constraints in Edge-Triggered Systems

If launching edge is late and receiving edge is early, the data will not be too late if:

$$T_{c-q} + T_{logic} + T_{SU} < T - T_{JS,1} - T_{JS,2} + \delta$$

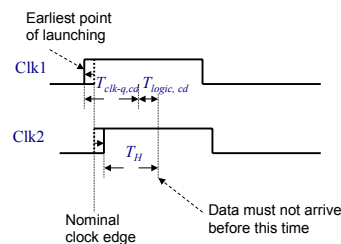
Minimum cycle time is determined by the maximum delays through the logic

$$T_{c-q} + T_{logic} + T_{SU} - \delta + 2 T_{JS} < T$$

Skew can be either positive or negative

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Shortest Path



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Clock Constraints in Edge-Triggered Systems

If launching edge is early and receiving edge is late:

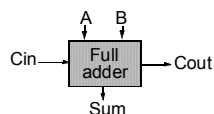
$$T_{c-q, cd} + T_{logic, cd} - T_{JS,1} > T_H + T_{JS,2} + \delta$$

Minimum logic delay

$$T_{c-q, cd} + T_{logic, cd} > T_H + 2T_{JS} + \delta$$

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Full-Adder



A	B	C _i	S	C _o	Carry status
0	0	0	0	0	delete
0	0	1	1	0	delete
0	1	0	1	0	propagate
0	1	1	0	1	propagate
1	0	0	1	0	propagate
1	0	1	0	1	propagate
1	1	0	0	1	generate
1	1	1	1	1	generate

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Express Sum and Carry as a function of P, G, D

Define 3 new variable which ONLY depend on A, B

Generate (G) = AB

Propagate (P) = A ⊕ B

Delete = $\overline{A} \overline{B}$

$$C_o(G, P) = G + PC_i$$

$$S(G, P) = P \oplus C_i$$

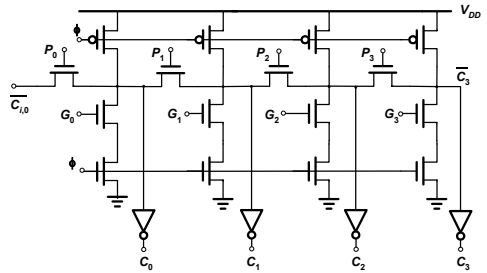
Can also derive expressions for S and C_o based on D and P

Note that we will be sometimes using an alternate definition for

Propagate (P) = A + B

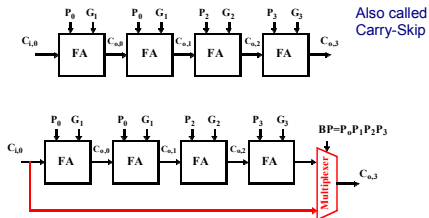
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Manchester Carry Chain



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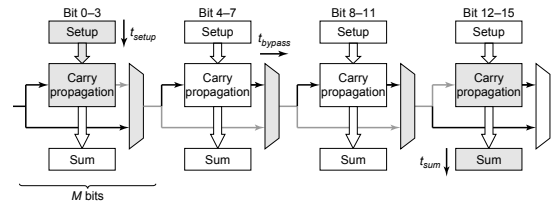
Carry-Bypass Adder



Idea: If (P0 and P1 and P2 and P3 = 1) then $C_{o3} = C_0$, else "kill" or "generate".

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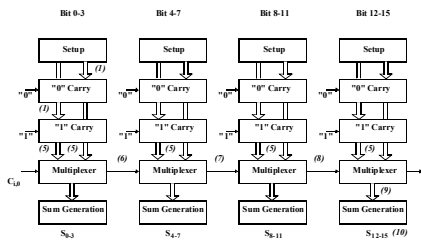
Carry-Bypass Adder (cont.)



$$t_{adder} = t_{setup} + M_{tcarry} + (N/M-1)t_{bypass} + (M-1)t_{tcarry} + t_{sum}$$

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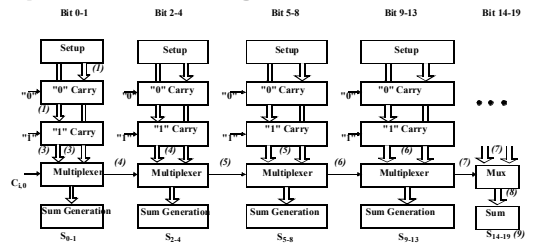
Linear Carry Select



$$t_{add} = t_{setup} + \left(\frac{N}{M}\right)t_{tcarry} + M t_{mux} + t_{sum}$$

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Square Root Carry Select



$$t_{add} = t_{setup} + P \cdot t_{tcarry} + (\sqrt{2N})t_{mux} + t_{sum}$$

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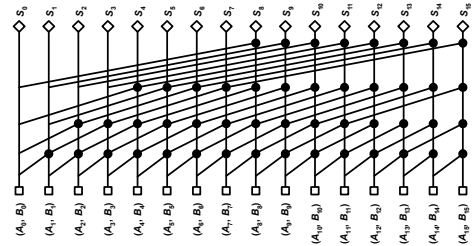
Carry Lookahead Trees

$$\begin{aligned}
 C_{0,0} &= G_0 + P_0 C_{i,0} \\
 C_{0,1} &= G_1 + P_1 G_0 + P_1 P_0 C_{i,0} \\
 C_{0,2} &= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{i,0} \\
 &= (G_2 + P_2 G_1) + (P_2 P_1)(G_0 + P_0 C_{i,0}) = G_{2,1} + P_{2,1} C_{0,0}
 \end{aligned}$$

Can continue building the tree hierarchically.

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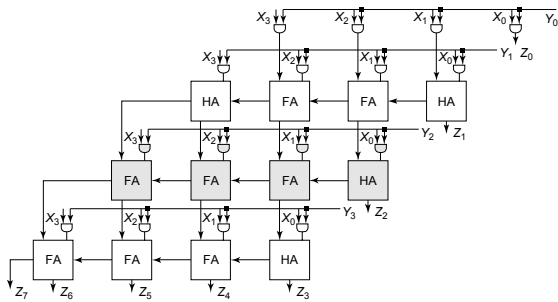
Tree Adders



16-bit radix-2 Kogge-Stone tree

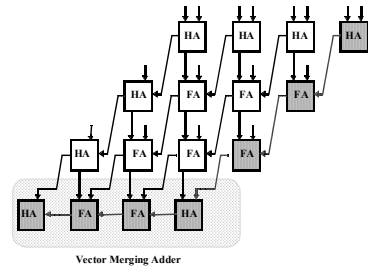
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The Array Multiplier



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Carry-Save Multiplier

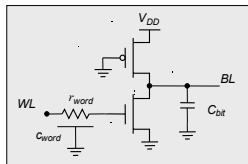


$$t_{mult} = (N-1) \cdot t_{carry} + (N-1) \cdot t_{and} + t_{merge}$$

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Equivalent Transient Model for MOS NOR ROM

Model for NOR ROM

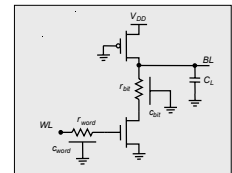


- Word line parasitics
 - Wire capacitance and gate capacitance
 - Wire resistance (polysilicon)
- Bit line parasitics
 - Resistance not dominant (metal)
 - Drain and Gate-Drain capacitance

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Equivalent Transient Model for MOS NAND ROM

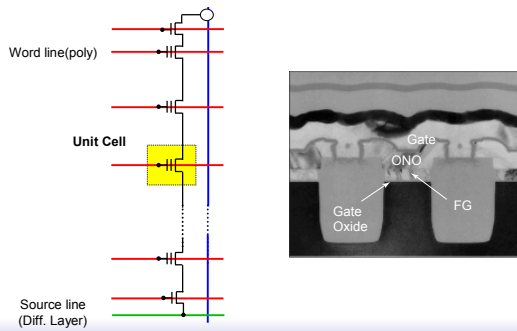
Model for NAND ROM



- Word line parasitics
 - Similar to NOR ROM
- Bit line parasitics
 - Resistance of cascaded transistors dominates
 - Drain/Source and complete gate capacitance

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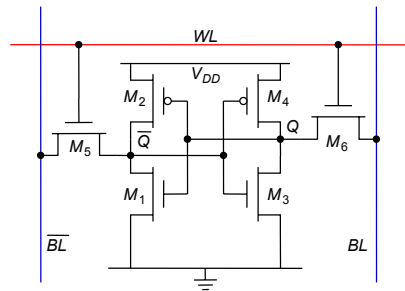
NAND Flash Memory



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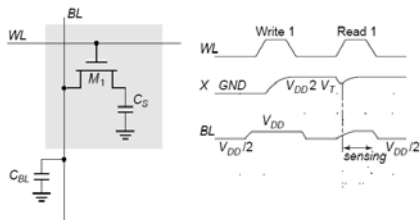
Courtesy Toshiba

6-transistor CMOS SRAM Cell



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1-Transistor DRAM Cell



Write: C_S is charged or discharged by asserting WL and BL.
Read: Charge redistribution takes place between bit line and storage capacitance

$$\Delta V = V_{BL} - V_{PRE} = V_{BIT} - V_{PRE} \frac{C_S}{C_S + C_{BL}}$$

Voltage swing is small; typically around 250 mV.

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